LISTING OF CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application:

Claims 1-24 (Canceled).

Claim 25 (Currently Amended): A voltage-driven power semiconductor device of a pressure-contact type, comprising:

a chip-like injection enhanced gate transistor (IEGT) having a collector on one side, and further having a main emitter, a current sense emitter electrically separated from the main emitter, a current sense terminal connected to the current sense emitter and configured to extract current flowing through the current sense emitter to an external protection circuit , a high-resistance base layer, and an MOS gate on an opposing side which opposes said one side, said MOS gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said MOS gate, a potential of said MOS gate being controlled according to an electric current passing through said current sense emitter via the protection circuit, electrical current from said collector being made to flow to both said main emitter and said current sense terminal, a carrier concentration in a current path defined between the main emitter and the collector having a maximum value at the opposing MOS gate side of the high-resistance base layer, and electron injection efficiency at said main emitter and said current sense emitter being 0.73 or more, the electron injection efficiency being defined by a ratio of an electron current and a total current consisting of the electron current and a hole current;

a plate-like collector press-contacting electrode terminal arranged on said one side of said IEGT and electrically connected to said collector in compression contact with the collector; and

a plate-like emitter press-contacting electrode terminal arranged on said opposing side of said IEGT and electrically connected to said main emitter in compression contact with the main emitter,

wherein said voltage-driven power semiconductor device is configured as a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

Claim 26 (Previously Presented): The voltage-driven power semiconductor device according to claim 25, wherein said gate is a trench-type gate embedded in said opposing side of said chip, and

carrier accumulation efficiency of said main emitter and said current sense terminal in an ON state is greater than that of an insulated gate bipolar transistor (IGBT).

Claim 27 (Currently Amended): A voltage-driven power semiconductor device of a pressure contact type, comprising:

a chip-like voltage-driven power semiconductor element having a collector on one side, a main emitter, a current sense emitter <u>electrically</u> separated from the main emitter, a

current sense terminal connected to the current sense emitter and configured to extract a current flowing through the current sense emitter to an external protection circuit, a high-resistance base layer, and ~~a~~ an MOS gate on an opposing side which opposes said one side, said MOS gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said MOS gate, a potential of said MOS gate being controlled according to an electric current passing through said current sense emitter via the protection circuit, a carrier concentration in a current path defined between the main emitter and the collector having a maximum value at the opposing MOS gate side of the high-resistance base layer, and electrical current from said collector being made to flow to both said main emitter and said current sense terminal;

a plate-like collector press contacting electrode terminal arranged on said one side of said power semiconductor device and electrically connected to said collector in compression contact with the collector; and

a plate-like emitter press contacting electrode terminal arranged on said opposing side of said power semiconductor device and electrically connected to said main emitter,

wherein said voltage-driven power semiconductor device is configured as a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

Claim 28 (Previously Presented): The voltage-driven power semiconductor device according to claim 27, wherein said power semiconductor element is an injection enhanced gate transistor (IEGT),

carrier accumulation efficiency of said main emitter and said current sense terminal in an ON state is greater than that of an insulated gate bipolar transistor (IGBT), and

electron injection efficiency at said main emitter and said current sense terminal is 0.73 or more.

Claim 29 (Currently Amended): A voltage-driven power semiconductor device of a pressure-contact type, comprising:

a plurality of voltage-driven power semiconductor elements connected in series and in parallel, said power semiconductor elements including semiconductor chips and said semiconductor chips having collectors on one side, main emitters, at least one current sense emitter electrically separated from the main emitter, at least one current sense terminal connected to the at least one current sense emitter and configured to extract a current flowing through the at least one current sense emitter to an external protection circuit, high-resistance base layers, and MOS gates on an opposing side which opposes said one side, said MOS gates being arranged on channel regions between said collectors and said main emitters with gate insulating films interposed between said channel regions and said MOS gates, potential of said MOS gates being controlled according to an electric current passing through said at least one current sense emitter, a carrier concentration in each current path defined between each of the main emitters and each of the collectors having a maximum value at each opposing MOS gate side of the high-resistance base layers, and electrical current from said collectors being made to flow to both said main emitters and said at least one current sense terminal;

a plate-like collector press-contacting electrode terminal arranged on said one side of said plurality of power semiconductor elements, and electrically connected to said collectors in compression contact with the collectors; and

a plate-like emitter press-contacting electrode terminal arranged on said opposing side of said plurality of power semiconductor elements and electrically connected to said main emitters in compression contact with the main emitters,

wherein said voltage-driven power semiconductor device is configured as a press-contacting type package,

said collectors of said power semiconductor elements are pressed by said plate-like collector press contacting electrode terminal so that said collectors and said collector electrode terminal are pressed to electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter press-contacting electrode terminal so that said main emitters and said emitter electrode terminal are pressed to be electrically connected together.

Claim 30 (Previously Presented): The voltage-driven power semiconductor device according to claim 29, wherein at least those power semiconductor elements connected in series have overvoltage protective circuits.

Claim 31 (Currently Amended): A voltage-driven power semiconductor device of a pressure-contact type comprising:

a plurality of voltage-driven power semiconductor elements connected in series and in parallel, said power semiconductor elements including semiconductor chips and said semiconductor chips having collectors on one side, main emitters, at least one current sense emitter electrically separated from the main emitter, at least one current sense terminal

connected to the at least one current sense emitter and configured to extract a current flowing through the at least one current sense emitter to an external protection circuit, high-resistance base layers, and MOS gates on an opposing side which opposes said one side, said MOS gates being arranged on channel regions between said collectors and said main emitters with gate insulating films interposed between said channel regions and said MOS gates, potential of said MOS gates being controlled according to an electric current passing through said at least one current sense emitter, a carrier concentration in each current path defined between each of the main emitters and each of the collectors having a maximum value at each opposing MOS gate side of the high-resistance base layers, electrical current from said collectors being made to flow to both said main emitters and said at least one current sense terminal, and said MOS gates being a trench-type gate embedded in said opposing side;

a plate-like collector pressing-contacting electrode terminal arranged on said one side of said plurality of power semiconductor elements, and electrically connected to said collectors in compression contact with the collectors; and

a plate-like emitter press-contacting electrode terminal arranged on said opposing side of said plurality of power semiconductor elements and electrically connected to said main emitters in compression contact with the main emitters;

wherein said voltage-driven power semiconductor device is configured as a press-contacting type package,

said collectors of said power semiconductor elements are pressed by said plate-like collector press-contacting electrode terminal so that said collectors and said collector electrode terminal are electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter press-contacting electrode terminal so that said main emitters and said emitter electrode terminal are electrically connected together.

Claim 32 (Previously Presented): The voltage-driven power semiconductor device according to claim 27, wherein said gate is a trench-type gate embedded in said opposing side.

Claim 33 (Currently Amended): A voltage-driven power semiconductor device of a pressure-contact type comprising:

a plurality of first injection enhanced gate transistor (IEGT) chips, each first IEGT chip having a collector on one side, and a main emitter on an opposite side, a high-resistance base layer and an MOS gate on the opposite side which opposes said one side, said MOS gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said MOS gate, electrical current from said collector being made to flow to said main emitter, a carrier concentration in a current path defined between the main emitter and the collector having a maximum value at an MOS gate side of the high-resistance base layer, and electron injection efficiency being defined by a ratio of an electron current and a total current consisting of the electron current and a hole current;

a second IEGT chip having a collector on one side, and a main emitter on an opposing side which opposes said one side, a current sense emitter electrically separated from the main emitter of the second IEGT chip, a current sense terminal connected to the current sense emitter and configured to extract a current flowing through the current sense emitter to an external protection circuit, a high-resistance base layer and an MOS gate on the opposing side, said MOS gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said MOS gate, a potential of said MOS gate being controlled according to an electric current passing

through said current sense emitter via the protection circuit, electrical current from said collector being made to flow to both said main emitter and said current sense terminal, a carrier concentration in a current path defined between the main emitter and the collector having a maximum value at an MOS gate side of the high-resistance base layer, and electron injection efficiency at said main emitter and said current sense emitter being 0.73 or more, the electron injection efficiency being defined by a ratio of an electron current and a total current consisting of the electron current and a hole current;

a plate-like collector electrode commonly press-contacting to the collectors of the first and second IEGT chips; and

a plate-like emitter electrode commonly press-contacting to the main emitters of the first and second IEGT chips and to the current sensing emitter of the second IEGT chip.

Claim 34 (Currently Amended): A voltage-driven power semiconductor device of a pressure-contact type comprising:

a plurality of injection enhanced gate transistor (IEGT) chips each having a collector on one side, a main emitter on an opposing side which opposes said one side, a current sense emitter electrically separated from the main emitter, a high-resistance base layer, and an MOS gate on the opposing side, said MOS gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said MOS gate, a carrier concentration in a current path defined between the main emitter and the collector having a maximum value at an MOS gate side of the high-resistance base layer, and electron injection efficiency at said main emitter and said current sense emitter being 0.73 or more, the electron injection efficiency being defined by a ratio of an electron current and a total current consisting of the electron current and a hole current;

a plate-like collector electrode commonly press-contacting to the collectors of the IEGT chips; and

a plate-like emitter electrode commonly press-contacting to the main emitters of the IEGT chips;

wherein a current sense emitter of at least one IEGT chip of the IEGT chips is connected to a current sense terminal configured to extract a current flowing through the current sense emitter of the at least one IIEGT chip to an external protection circuit so that an electrical current from said collector is made to flow to both said main emitter and said current sense terminal, and a potential of said MOS gate is controlled according to an electric current passing through said current sense emitter via the protection circuit.